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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,427	09/28/2006	Seiichi Tamura	03500.109226.	8692
	7590 04/02/200 CELLA HARPER &	EXAMINER		
30 ROCKEFELLER PLAZA			CHIU, TSZ K	
NEW YORK, NY 10112			ART UNIT	PAPER NUMBER
			2822	
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			04/02/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)			
	10/599,427	TAMURA ET AL.			
Office Action Summary	Examiner	Art Unit			
	Tsz K. Chiu	2822			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).			
Status					
Responsive to communication(s) filed on <u>27 Ar</u> This action is FINAL . 2b) ☑ This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4) Claim(s) 1-6 is/are pending in the application. 4a) Of the above claim(s) is/are withdrav 5) Claim(s) is/are allowed. 6) Claim(s) 1-6 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers 9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) access	r election requirement.	- - - - -			
Applicant may not request that any objection to the orection. Replacement drawing sheet(s) including the correction. 11) The oath or declaration is objected to by the Ex	drawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). sected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 2/26/08.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	nte			

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1-6 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Prior Art (figure. 7 and 8).

With respect to claim 1, Applicant's Prior Art discloses

a first semiconductor region (18) of a first conductivity type for providing said photoelectric conversion device (figure. 8)

a second semiconductor region (12) of a second conductivity type that is same conductivity type of said signal charge; and

a third semiconductor region (CMOS device one of the source/drain region, shown in figure. 7) of the first conductivity type for providing said peripheral circuit;

Applicant's Prior Art does not discloses there is impurity concentration of said first semiconductor region is higher than the impurity concentration of said second semiconductor region.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the different impurity concentration in one region than the other region, since it has been held that where the general conditions of a

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claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. (1955)

With respect to claim 2, Applicant's Prior Art discloses

a first semiconductor region (18) of a first conductivity type for providing said photoelectric region (figure. 8),

a second semiconductor region (12) of a second conductivity type that is same conductivity type of said signal charge; and

a third semiconductor region (CMOS device one of the source/drain region, shown in figure. 7) of the first conductivity type for providing said peripheral circuit;

wherein said first and third semiconductor regions comprise impurity concentration peaks. Applicant's Prior Art does not discloses there is impurity concentration of said first and third semiconductor region comprise impurity concentration peaks.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the different impurity concentration in one region than the other region, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. (1955)

With respect to claim 3-4, Applicant's Prior Art discloses invention set forth to claim 1, however Applicant's Prior Art did not discloses the different impurity concentration between the photoelectric device and the CMOS device however, it would have been obvious to one having ordinary skill in the art at the time the invention

was made to have the different impurity concentration in one region than the other region, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. (1955)

With respect to claim 5-6, Applicant's Prior Art discloses first semiconductor region (18) has a structure wherein plural semiconductor regions having impurity concentration peaks are disposed in a depth direction inside said substrate (11, For example Fig. 8), and the impurity concentration of the impurity concentration peak formed in the deepest portion is higher-than the impurity concentration of the impurity concentration peak formed at said photoelectric conversion device side, however, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the different impurity concentration in one region than the other region, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. (1955)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/ Supervisory Patent Examiner, Art Unit 2822

TC